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(54) Reduction of aperture distortion in parallel A/D converters

(57) A method and circuit for improving the aperture distortion in parallel A/D converters by reducing the delay mismatch in the sample-and-hold portion of an converter circuit. The technique involves generating two complementary clocks. Q and $\overline{Q}$, from a single master clock and then gating these two clocks, in a random fashion, with the original master clock in order to significantly reduce the delay mismatch in the circuit. This approach involves the random selection of gated switches from dual banks 50,60 each containing a plurality of parallel switches 51-54,61-64 and then gating the output of these randomly selected switches with the master clock in dual banks 70,80 of master clock gated switches 71-74,81-84, thereby compensating for aperture error by converting any systematic aperture mismatch between the sampling clocks into random noise spread over the frequency band. High speed A/D converters incorporating the techniques of this invention will provide superior performance in digital audio, digital video, and many other digital applications.

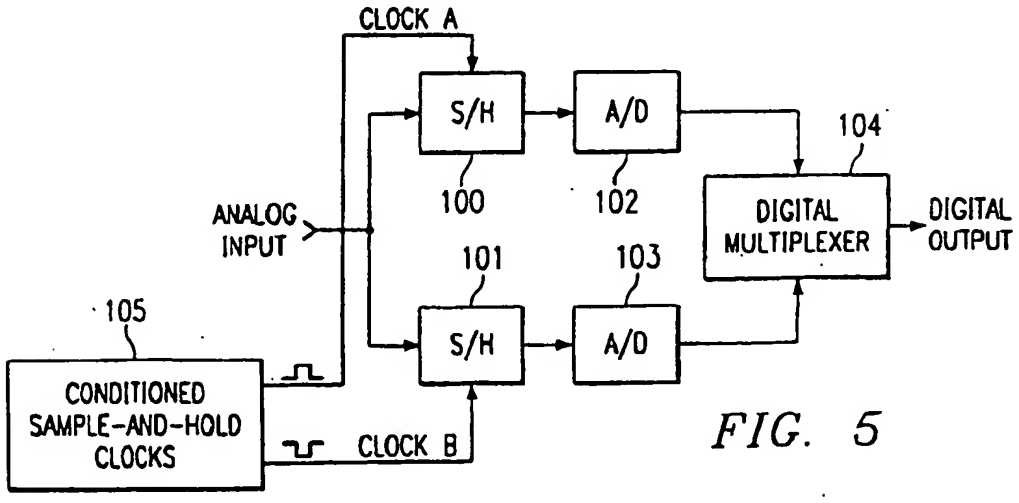

FIG. 5

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Description

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention relates to analog-to-digital (A/D) converter circuits and more specifically to the reduction of aperture distortion in parallel circuits of this type by conditioning of the sample-and-hold clocks.

DESCRIPTION OF THE RELATED ART

[0002] Figure 1a shows a typical block diagram for a two channel parallel A/D converter circuit. In this circuit, the analog input signal is directed along two parallel data paths, each consisting of a sample-and-hold (S/H) circuit in series with an analog-to-digital converter circuit; i.e., one path comprised of S/H 10 in series with A/D 12 and the other path comprised of S/H 11 in series with A/D 13. The two paths are then coupled to a digital multiplexer 14 where the signals are recombined to provide the digital output. The analog input signal is sampled in an odd-even fashion within the two signal paths by means of sample-and-hold clocks, Clock A and Clock B.

[0003] Figure 1b shows the timing diagram for the typical two channel A/D converter circuit of Figure 1a. Clock A is the clock for one of the parallel channel sample-and-hold circuits and Clock B is the clock for the other parallel channel sample-and-hold circuit, with Clock A and Clock B being complementary. Typically, the analog signal V_{in} is sampled on the trailing or negative edge of these clock pulses, as shown, alternating between Clock A and Clock B. Ideally, the high-to-low sampling edge of the clocks should be exactly $\frac{1}{f}$ apart in time, where T is the period of the clock pulse. However, in practice this is normally not the case due to the delay mismatch of the circuit parameters which can result in the presence of intermodulation tones in the sampled signal, given by $fin \pm \frac{fs}{2}$; where fs is the sampling frequency.

[0004] Typically, in attempting to minimize this circuit mismatch, a method of generating the complementary sample-and-hold clock signals from a single master clock, as shown in Figure 2, is used. Here, the complementary Clock A and Clock B signals are generated, by means of a divide-by-2 flip-flop 20 circuit, from a master clock signal. However, the drawback of this simple approach is that of signal delay, caused by component mismatching in the divide-by-2 flip-flop 20, which can result in significant delay between Clock A and Clock B, resulting in aperture distortion in the A/D converter.

[0005] One approach for improving the delay mismatch in the above circuit is to recombine the generated complementary clocks with the master clock by means of gating the two together, as shown in Figure 3, in order to remove some of the delay mismatch. In operation, the circuit generates two complementary sample-and-hold clocks, Clock A and Clock B, from a single master clock signal. The circuit is comprised of a flip-flop (F/F) 30 and two transmission gates (gated switches) 31-32. The complementary outputs, Q and $\overline{Q}$, of flip-flop 30 are connected, respectively, to the inputs of the two gated switches 31-32. A master clock (Clk) is connected to the input of flip-flop 30 and to the gates of switches 31-32. Finally, the outputs of the gated switches 31-32 provide the conditioned Clock A and Clock B sample-and-hold signals. In this circuit, the delay mismatch introduced by flip-flop 30 is effectively removed by gating the two flip-flop 30 output signals, Q and $\overline{Q}$, again with the master clock by means of the two gated switches 31-32. However, there is some amount of delay mismatch introduced between the two signals by the two transmission gates 31-32 themselves, although this mismatch can be minimized and somewhat controlled by matching the threshold of the gates and by maintaining the overall circuit time constant at a minimum. These factors can be addressed during the design of the integrated circuit.

[0006] The new approach of this invention addresses the drawbacks of the above circuits and significantly improves the aperture distortion problem found in many typical parallel A/D converter circuits.

SUMMARY OF THE INVENTION

[0007] In accordance with the present invention, there is provided a method for reducing the aperture distortion in parallel A/D converters by randomizing the delay mismatch in the sampling portion of the circuit.

[0008] In accordance with the present invention, there is also provided a circuit for minimizing the delay mismatch in complementary sample-and-hold clocks by providing a plurality of randomly selected parallel paths through which the two generated complementary signals are gated with an original master clock.

[0009] In combination with a parallel analog-to-digital converter circuit wherein parallel signal paths are sampled alternately by means of complementary sample-and-hold clocks, the invention may provide:

the conversion of systematic aperture mismatch in the circuit to random noise distributed over a broad band of frequencies;

a method for reducing the aperture distortion in said parallel A/D converter by reducing the delay mismatch in the sampling portion of said circuit;

a circuit which produces said sample-and-hold clock with further reduced delay mismatch by providing a plurality of randomly selected parallel paths through which the two generated complementary signals are gated with the original master clock and may also provide:

a first sample-and-hold circuit in series with a first analog-to-digital circuit and in parallel with a second sample-and-hold circuit in series with a second analog-to-digital circuit;

- a digital multiplexer circuit, and
- randomly generated complementary sample-and-hold clocks.

[0010] A method and circuit for reducing the aperture distortion in parallel A/D converters by improving the delay mismatch in the sample-and-hold stages of the circuit is disclosed. The technique involves generating two complementary sample-and-hold signals, Q and $\overline{Q}$, from a single master clock and then gating them again with the original master clock in a random fashion to significantly reduce delay mismatch between them, thereby improving the aperture distortion in the circuit. It is the random nature of the approach that constitutes this invention.

[0011] In this approach, the sample-and-hold circuit's delay mismatch is further reduced by providing a plurality of randomly selected parallel paths for gating the generated complementary signals, Q and $\overline{Q}$, with the master clock. These parallel paths may each consist of a randomly selected switch in series with a master clock switch. This technique tends to convert any systematic aperture mismatch between the two generated complementary clocks, Clock A and Clock B, into random noise which is spread over a wide band of frequencies.

[0012] High speed parallel A/D converters utilizing the sample-and-hold aperture distortion reduction techniques of this invention are used in, but are not limited to, such applications as:

1) video signal processing,
2) video bandwidth compression,
3) digital video transmission/reception,
4) digital audio processing,
5) digital image enhancement,
6) radar signal analysis, and
7) others.

DESCRIPTION OF THE VIEWS OF THE DRAWINGS

[0013] The included drawings are as follows:

Figure 1a is a block diagram for a typical two channel parallel A/D converter. (related art)

Figure 1b is the timing diagram for the two channel parallel A/D converter of Figure 1a. (related art)

Figure 2 is a block diagram for generating two complementary clock signals from a single master clock. (related art)

Figure 3 is a block diagram showing a typical approach for generating complementary sample-and-hold clocks with reduced aperture distortion for use in parallel A/D converter circuits. (related art)

Figure 4a is a block diagram showing the method of generating conditioned complementary sample-and-hold clocks as used in the preferred embodiment of this invention for significantly reducing the aperture distortion in parallel A/D converter circuits.

Figure 4b is a schematic for implementing the circuit of Figure 4a using MOS transistors.

Figure 5 is a block diagram of a parallel analog-to-digital converter which incorporates the conditioned complementary sample-and-hold clocks of this invention.

DETAILED DESCRIPTION

[0014] The present invention discloses techniques for reducing the aperture distortion in parallel A/D converter circuits by improving the delay mismatch in the sample-and-hold stages of the circuit.

[0015] Figure 4a shows a preferred embodiment which significantly improves the delay mismatch in the circuit by randomizing the aperture error. Here, a plurality of parallel gated switch paths are provided and are chosen randomly so as to effectively reduce the delay mismatch in the gates. The circuit is comprised of a divide-by-2 flip-flop 40 which generates complementary output signals, Q and $\overline{Q}$, from a master clock input signal (Clk). The Q and $\overline{Q}$ outputs of the flip-flop 40 are coupled to the inputs of two banks 50 and 60 of randomly gated switches, 51-54 and 61-64, respectively. The output of these randomly gated switches are connected to the corresponding inputs of the two banks 70 and 80 of master clock gated switches 71-74 and 81-84, respectively, all of which are clocked at the master clock rate, as indicated. The outputs of the gated switches 71-74 are coupled together to provide the Clock A sample-and-hold signal. Similarly, the outputs of the gated switches 81-84 are coupled together to provide the Clock B sample-and-hold signal. Finally, a random data generator 90 generates the random clock signals for enabling the random gated switches in banks 50 and 60. This random data generator can have individual gate signals for each of the random gated switches or can be used to supply the random gate signals between the two banks of switches in pairs; e.g., the gates of random gate switches 53 and 63 are driven from the same random gate signal. Although the switch banks are shown to have 4 gated switches each, this approach can be expanded by adding additional gated switches, as required, for finer reduction of aperture distortion, as illustrated. In operation, one or more of the parallel paths are randomly selected, under control of the random data generator 90, for both the Q and $\overline{Q}$ signals during each cycle. As a result, any systematic aperture mismatch between the sample-and-hold clocks, Clock A and Clock B, is converted into random noise which is distributed over a band of frequencies rather than appearing as discrete intermodulation tones in the clock signals.

[0016] Figure 4b shows the sample-and-hold complementary circuit of Figure 4a implemented using MOS transistors. All the switches 51-54, 61-64, 71-74, and

81-84, can be implemented with MOS or bipolar switch technology.

[0017] Figure 5 is a block diagram for a parallel analog-to-digital converter with conditioned complementary sample-and-hold clocks generated by the method of this invention. Here a typical parallel A/D converter, comprised of two parallel signal paths each consisting of a sample-and-hold circuit 100/101 and an A/D converter circuit 102/103 in series and a digital multiplexer 104 where the two signals are recombined at the output, has added a circuit 105 for conditioning the sample-and-hold clocks. In operation, the analog input signal is sampled in an odd-even fashion in the two paths, digitized, and then recombined in the digital multiplexer to provide the high speed digital output signal. The effects of the disclosed novel approach is to significantly improve the aperture distortion in the parallel A/D converter by reducing the delay mismatch in the sampling stages of the circuit by means of the sample-and-hold conditioning circuitry.

[0018] While the invention has been described in the context of preferred embodiments, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume embodiments other than that specifically set out and described above. Accordingly it is intended by the appended claims to cover all modifications of the invention which falls within the scope of the invention as defined in the appended claims.

Claims

1. A method for reducing the aperture distortion in parallel A/D converters by randomizing the delay mismatch in the sampling portion of the circuit.

2. The method of Claim 1, comprising:
the randomization of said aperture distortion by randomly selecting one or more of a plurality of parallel complementary output paths, each gated with said master clock, to provide complementary sample-and-hold clocks with reduced delay mismatch.

3. The method of Claim 2, further comprising:
the conversion of systematic aperture mismatch between said complementary sample-and-hold clocks into random noise distributed over a broad band of frequencies.

4. A circuit for minimizing the delay mismatch in complementary sample-and-hold clocks by providing a plurality of randomly selected parallel paths through which the two generated complementary signals are gated with an original master clock.

5. The circuit of Claim 4, comprising:

a flip-flop circuit;
a random data generator;
a first and second bank of randomly selected gated switches each comprising a plurality of parallel switch elements having randomly selectable gates;
a first and second bank of master clock gated switches each comprising a plurality of parallel switch elements having non-selectable gates;
the outputs of said first and said second bank of said master clock gated switches respectively coupled together to produce a first and a second sample-and-hold clock signal.

6. The circuit of Claim 5, wherein said first and second sample-and-hold clocks are complementary.

7. The circuit of Claim 5 or claim 6, wherein said random gated switches and said master clock gated switches are MOS transistors.

8. The circuit of any one of Claims 5 to 7, wherein:

first and second outputs of said flip-flop circuit are respectively coupled to inputs of first, second, third, and fourth gated switches in said first and second banks of randomly gated switches;
outputs of said first, second, third, and fourth gated switches in the said respective first and second banks of randomly gated switches are coupled to respective first, second, third, and fourth inputs of said gated switches in said first and second banks of master clock gated switches;
outputs of said first, second, third, and fourth gated switches in said first and second banks of master clock gated switches are coupled together to provide the said first and second sample-and-hold output clock signals; and
the said master clock signal is coupled to the input of said flip-flop circuit and to all gates of said first and second banks of said master clock gated switches.

9. The circuit of Claim 8, wherein first, second, third, and fourth outputs of said random data generator are coupled to the respective gates of said first, second, third, and fourth gated switches in the said first and second banks of random gated switches, respectively.

10. The circuit of Claim 8, wherein:

first, second, third, and fourth outputs of said random data generator are coupled to the respective gates of said first, second, third, and fourth gated switches in the said first bank of random gated switches; and
fifth, sixth, seventh, and eighth outputs of said

random data generator are coupled to the respective gates of said first, second, third, and fourth gated switches in the said second bank of random gated switches.

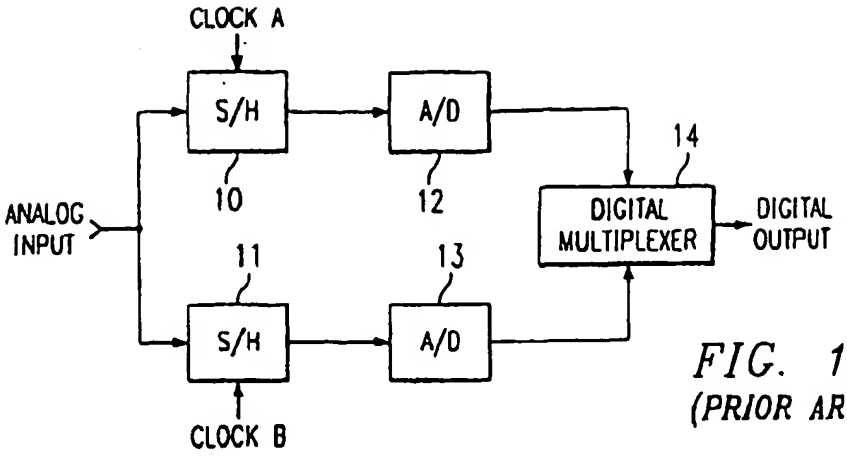


FIG. 1a
(PRIOR ART)

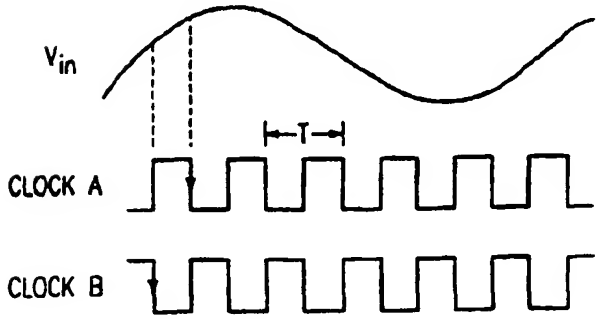


FIG. 1b
(PRIOR ART)

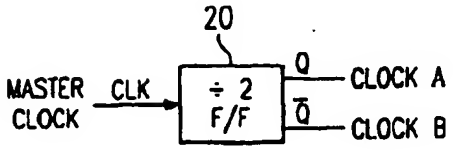


FIG. 2
(PRIOR ART)

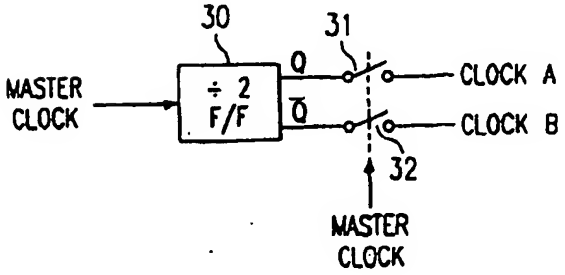


FIG. 3
(PRIOR ART)

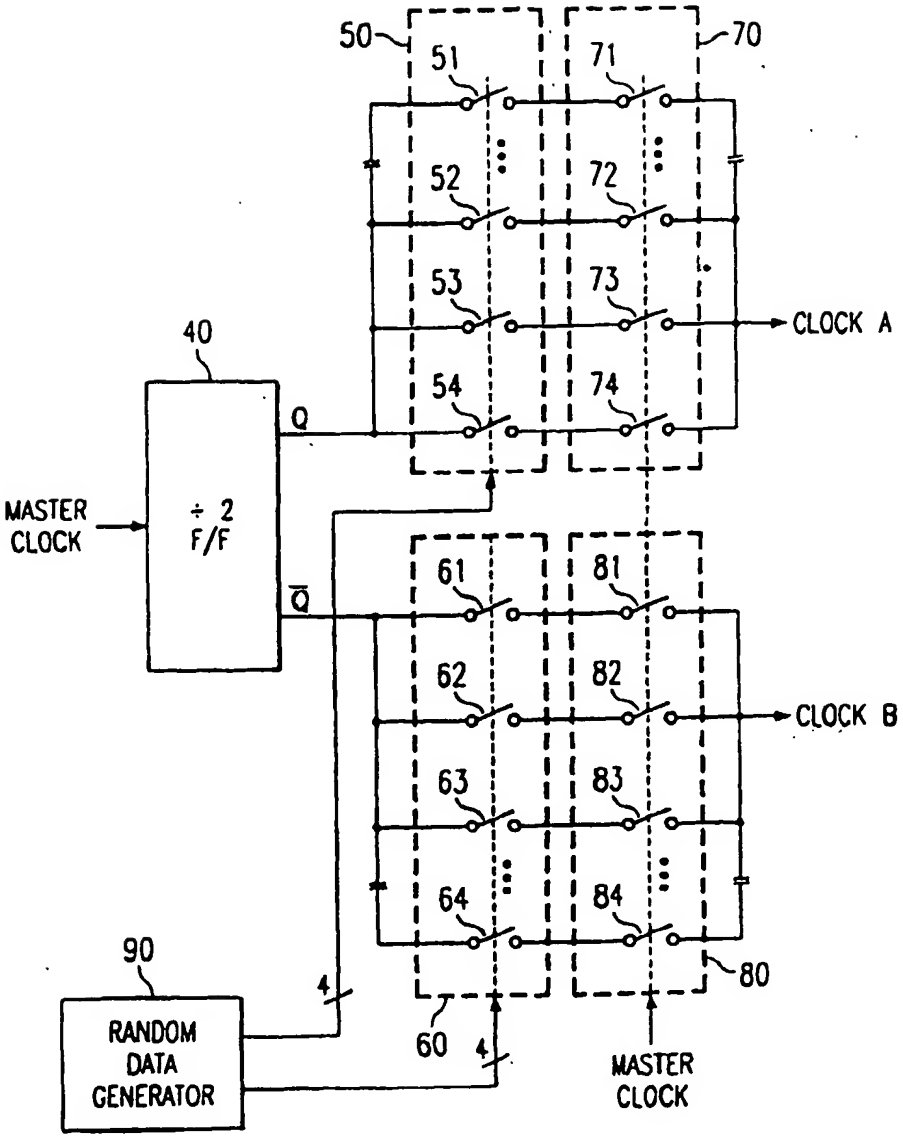
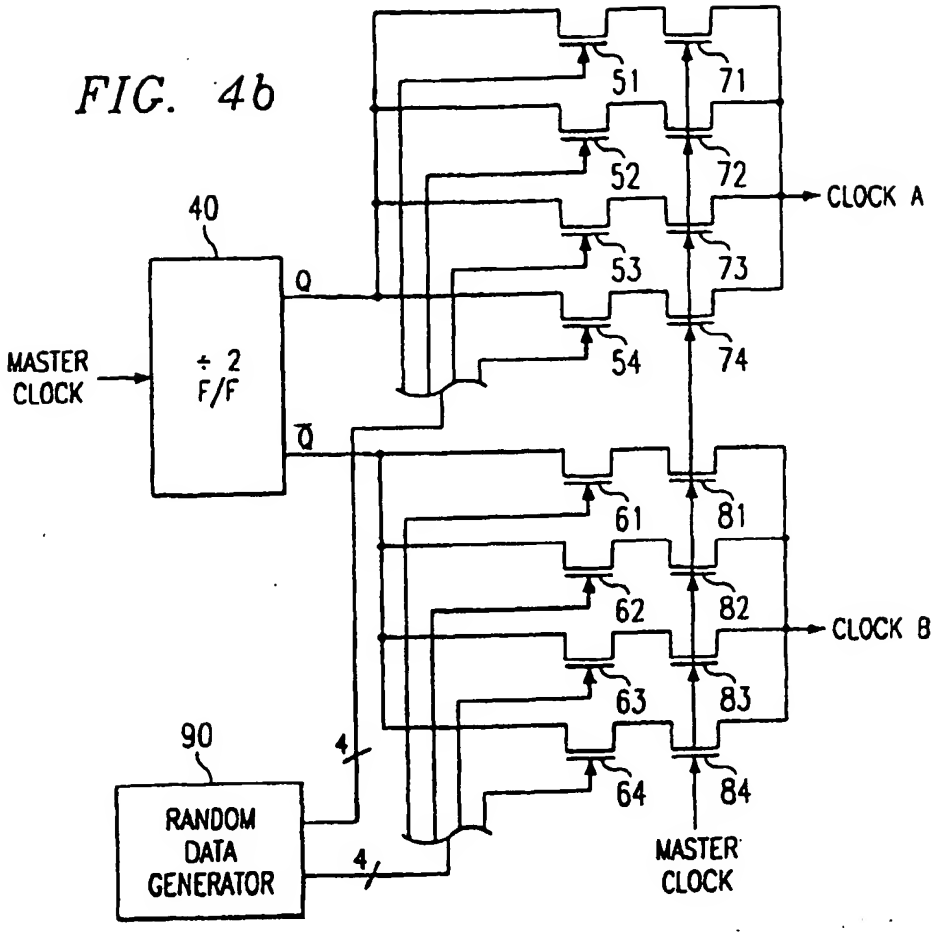


FIG. 4a

FIG. 4b



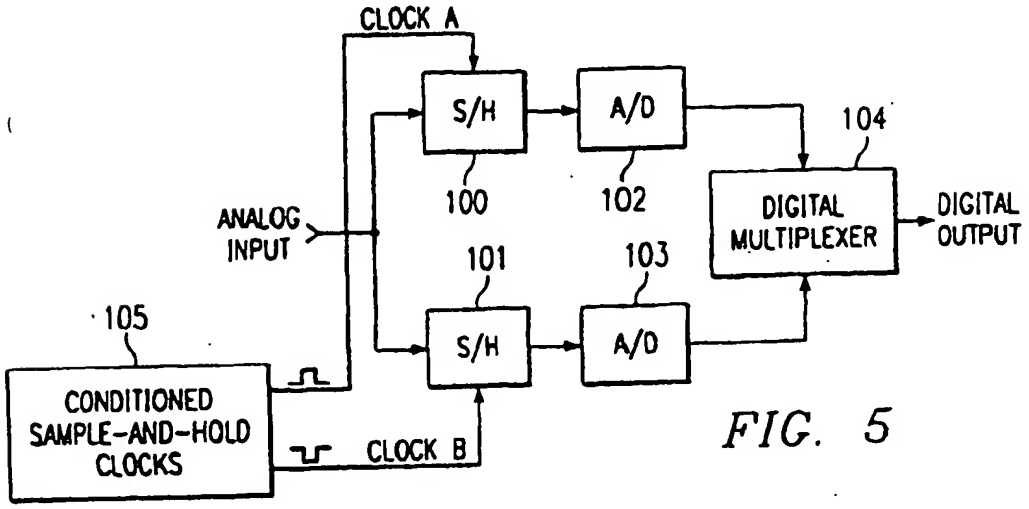


FIG. 5

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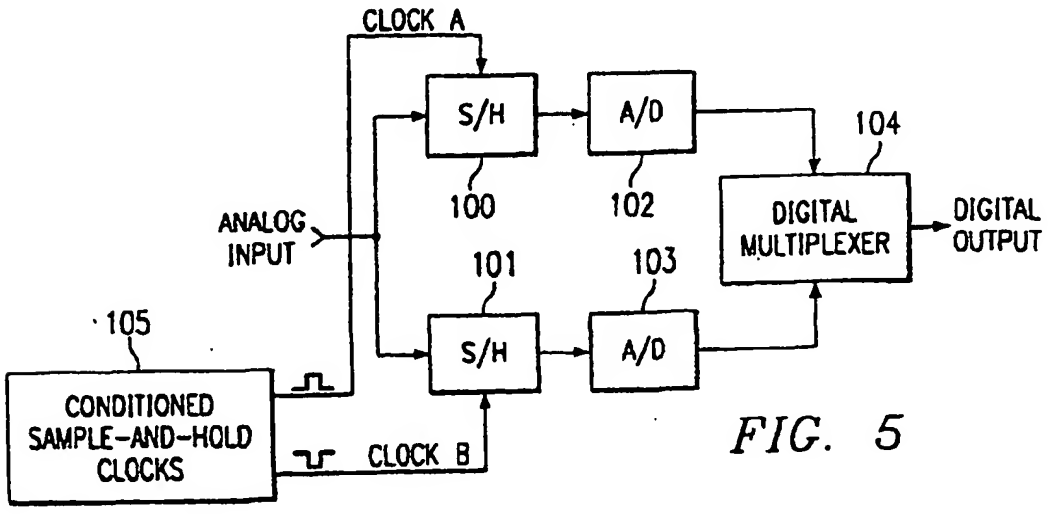

FIG. 5

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EUROPEAN SEARCH REPORT

Application Number
EP 00 30 2962

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	25 April 2003	Nicolaucig, A

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EUROPEAN SEARCH REPORT

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